

A 128 x 128 x 24Gb/s Crossbar,
Interconnecting 128 tiles in a single hop,
and Occupying 6% of their area

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presentation by
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- Motivation:

- Through real ASIC design
- Area cost estimation of high-valency crossbar datapaths

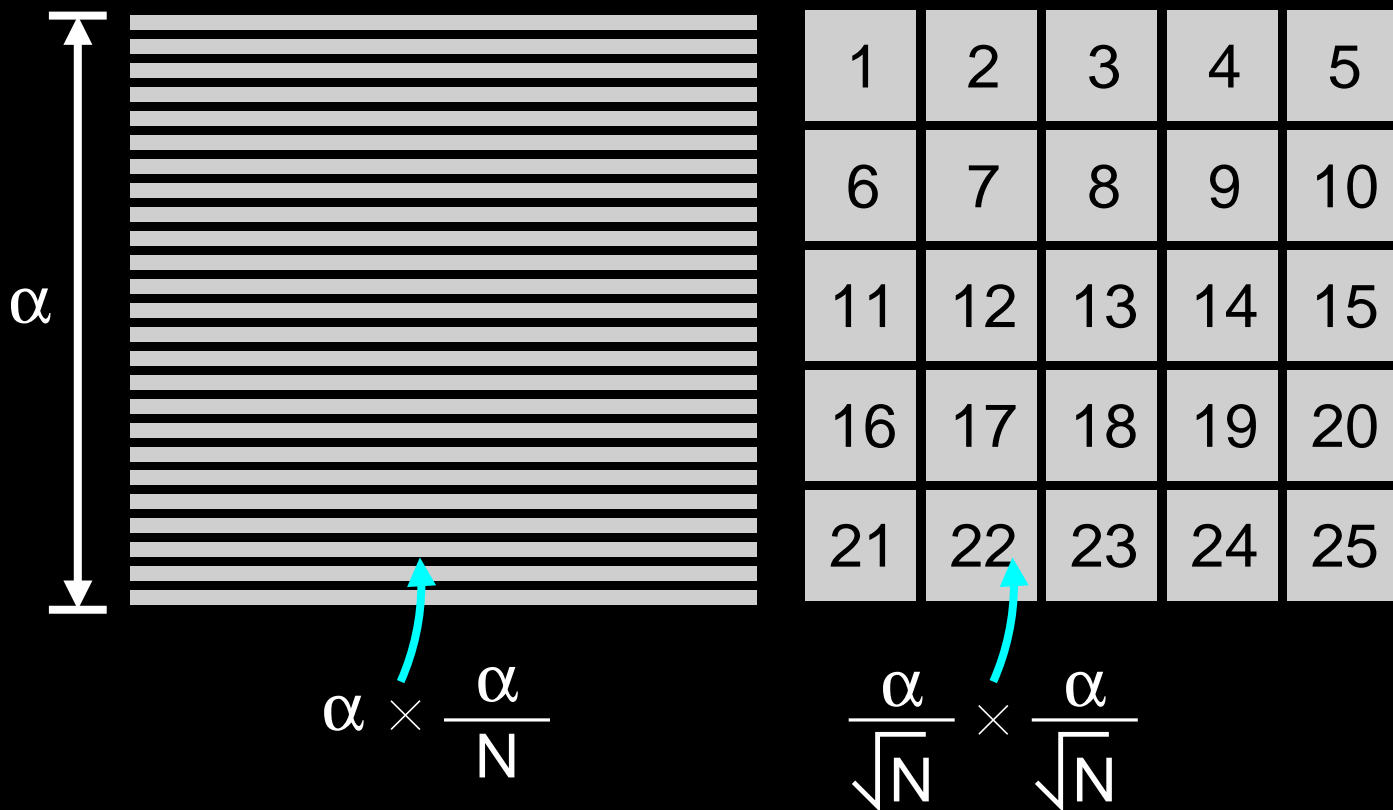
- Applications:

- Combined input-output queued switches (off chip)
- CMP crossbars (on chip)

- Contributions:

- A systematic design methodology
- Proof that a 128x128x24Gb/s crossbar will occupy < 6% of a typical die
- Crossbar area scales linearly --not quadratically-- with word width

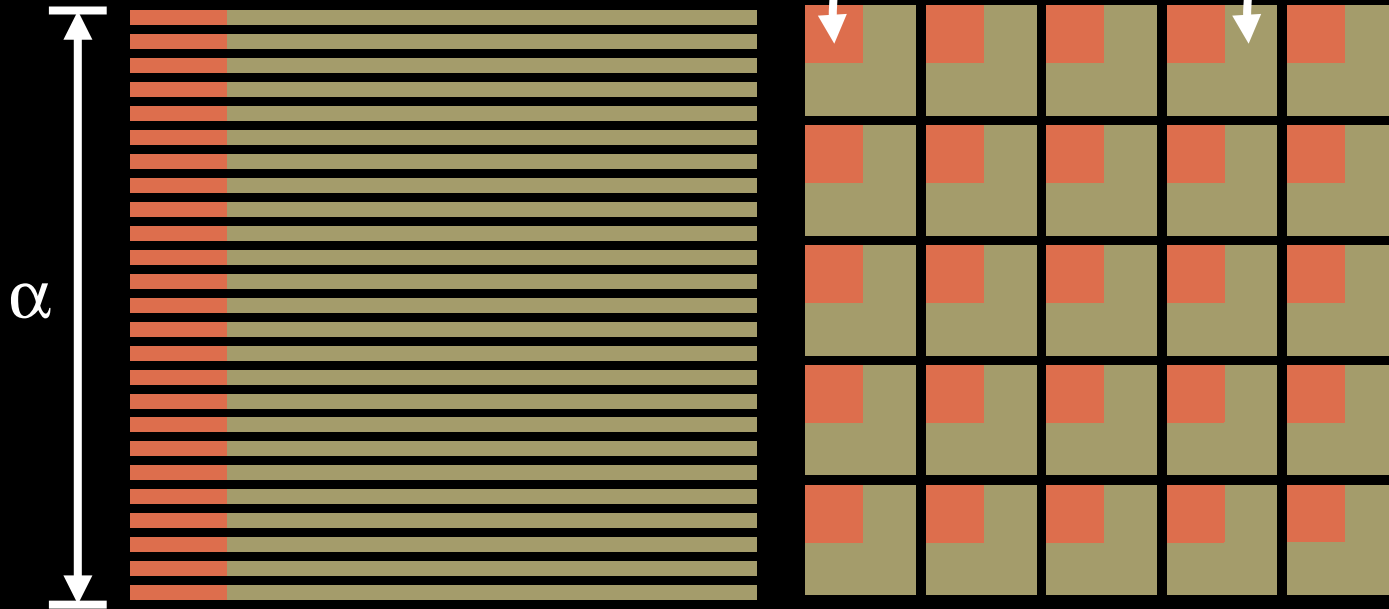
Floorplan Alternatives for a 25x25 Crossbar NoC



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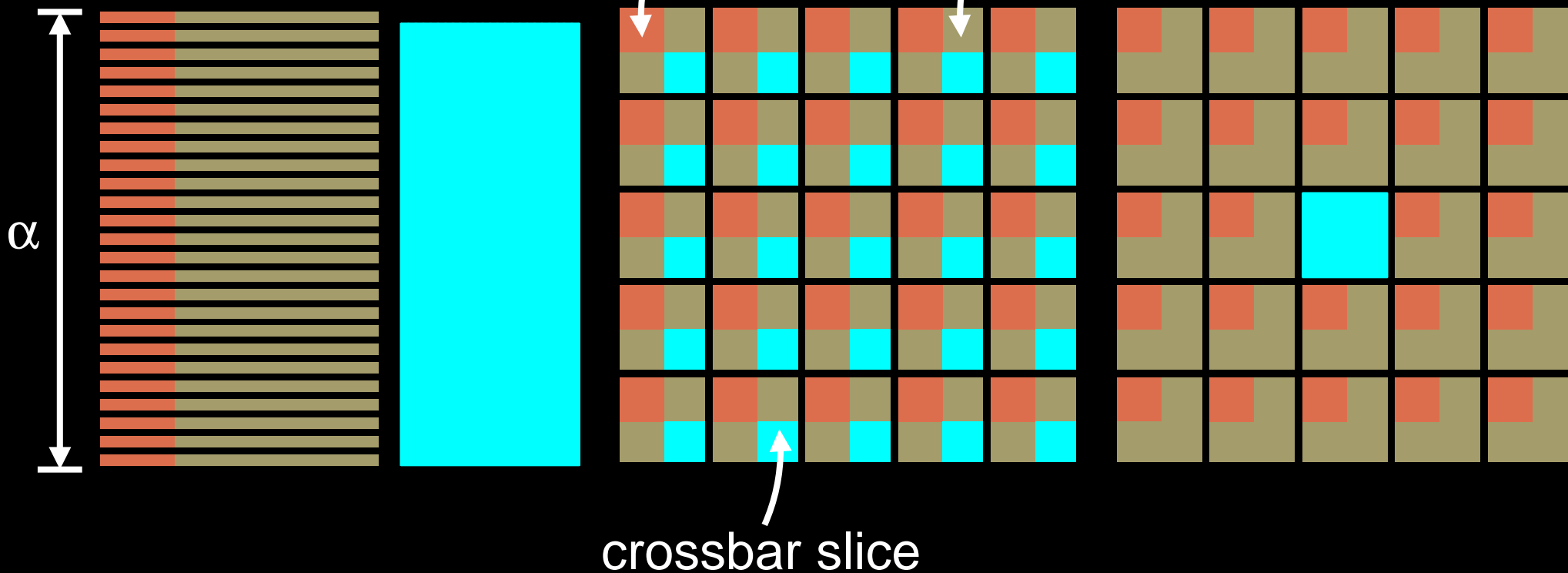
processor / switch–port control

memory / switch queues



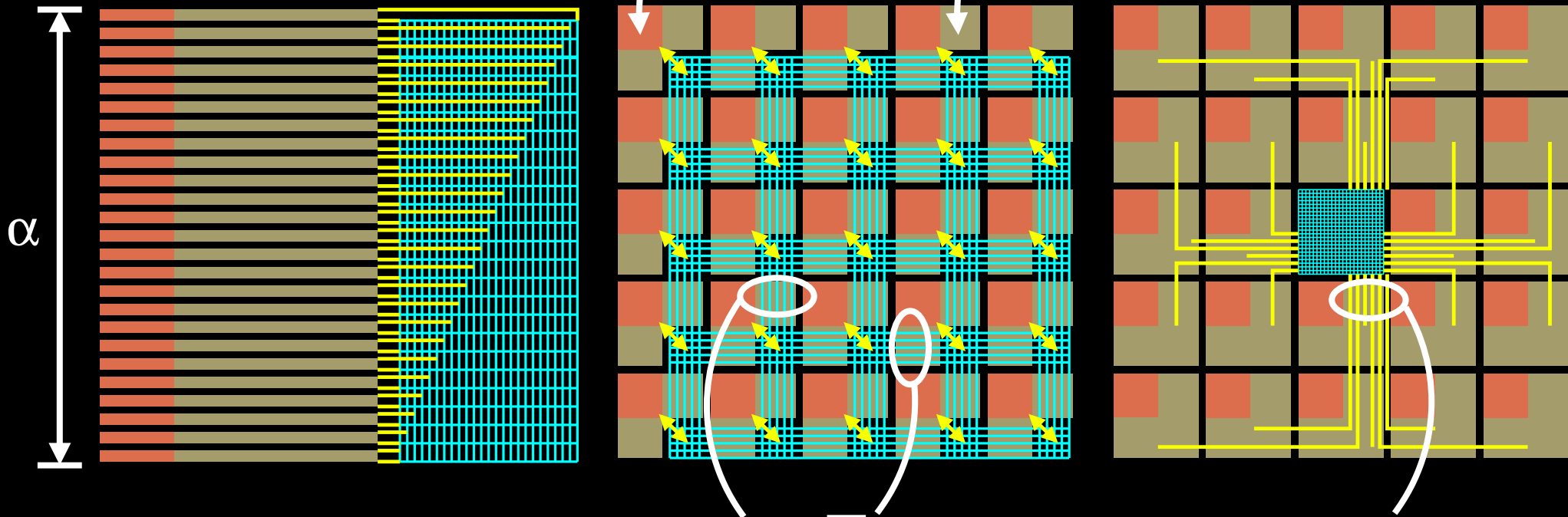
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lines on top of memory: $5 (= \sqrt{N})$

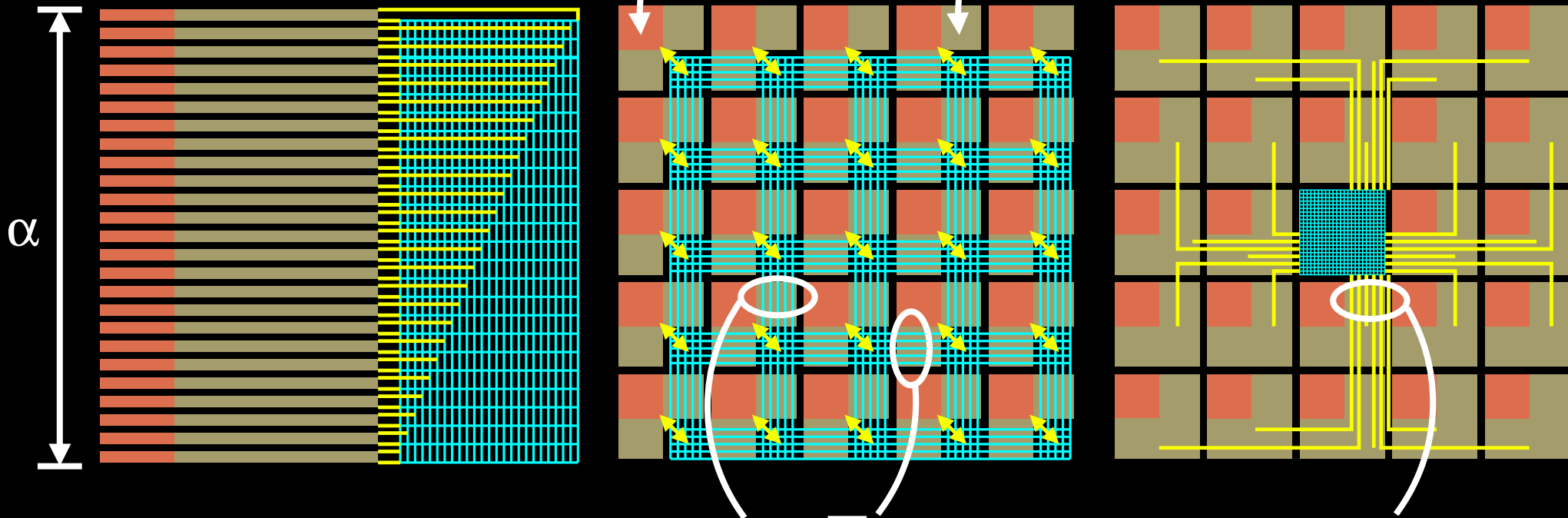
& total line length: $50\alpha (= 2N\alpha)$

$6 (= N/4)$

$25\alpha (= N\alpha)$

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lines on top of memory: 5 ($= \sqrt{N}$)

6 ($= N/4$)

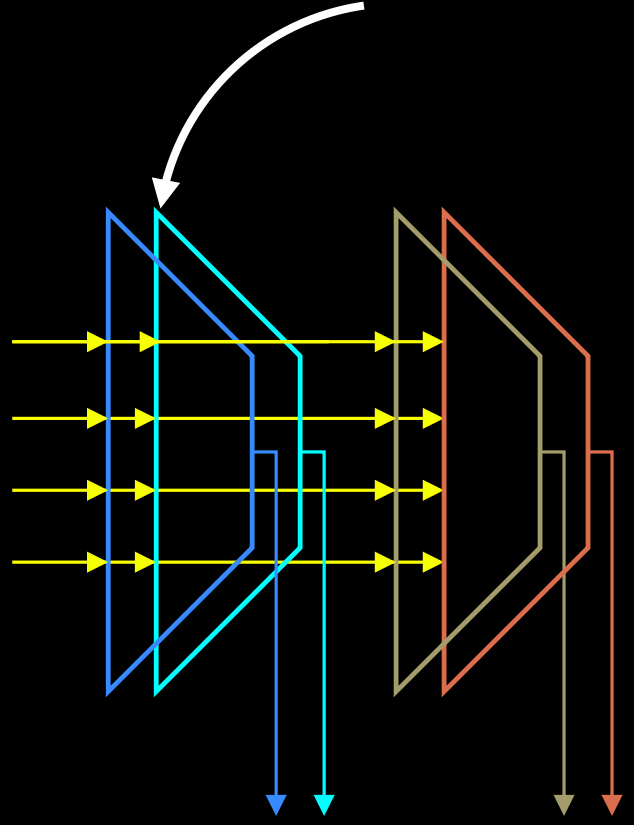
& total line length: 50α ($= 2N\alpha$)

25α ($= N\alpha$)

These are floorplans for a 25x25, not a 5x5 crossbar

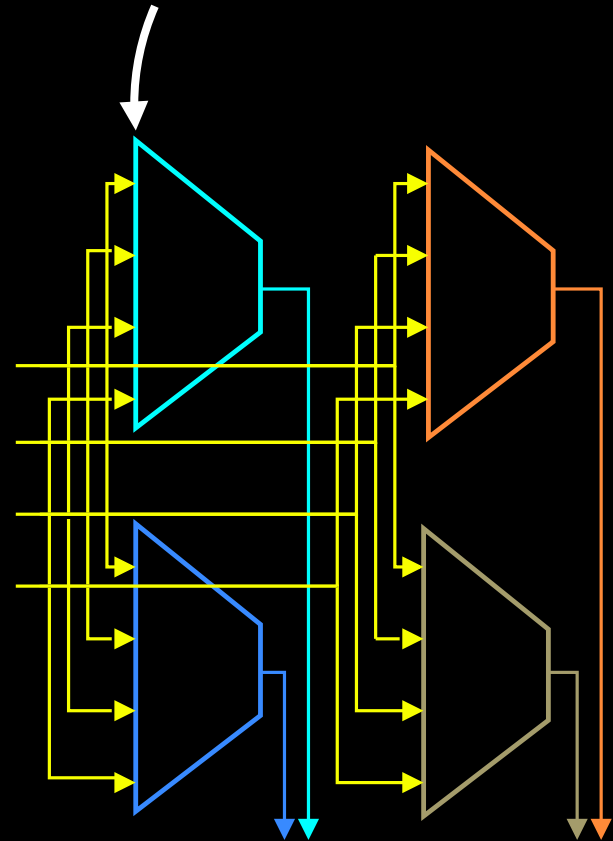
Floorplan Alternatives for a Centralized 2-bit 4x4 Crossbar

2-bit 4-to-1 mux



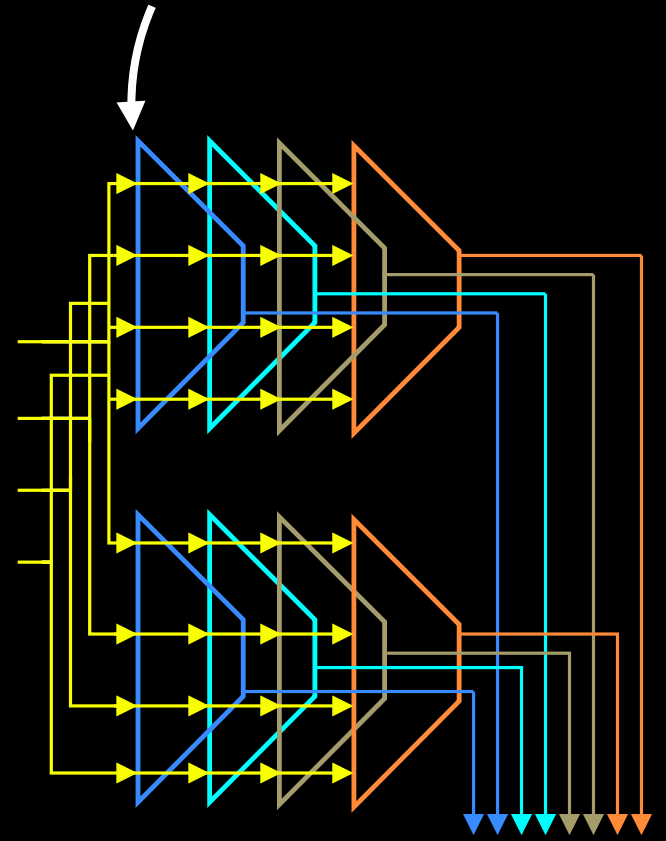
too slow

2-bit 4-to-1 mux



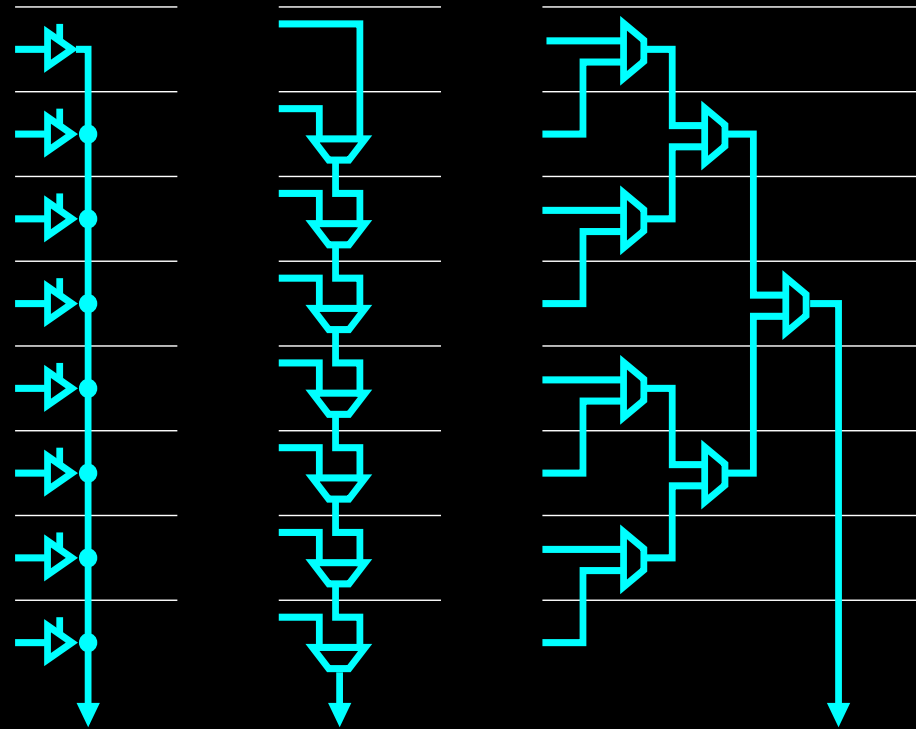
$O(N^2W)$ wires

1-bit 4-to-1 mux



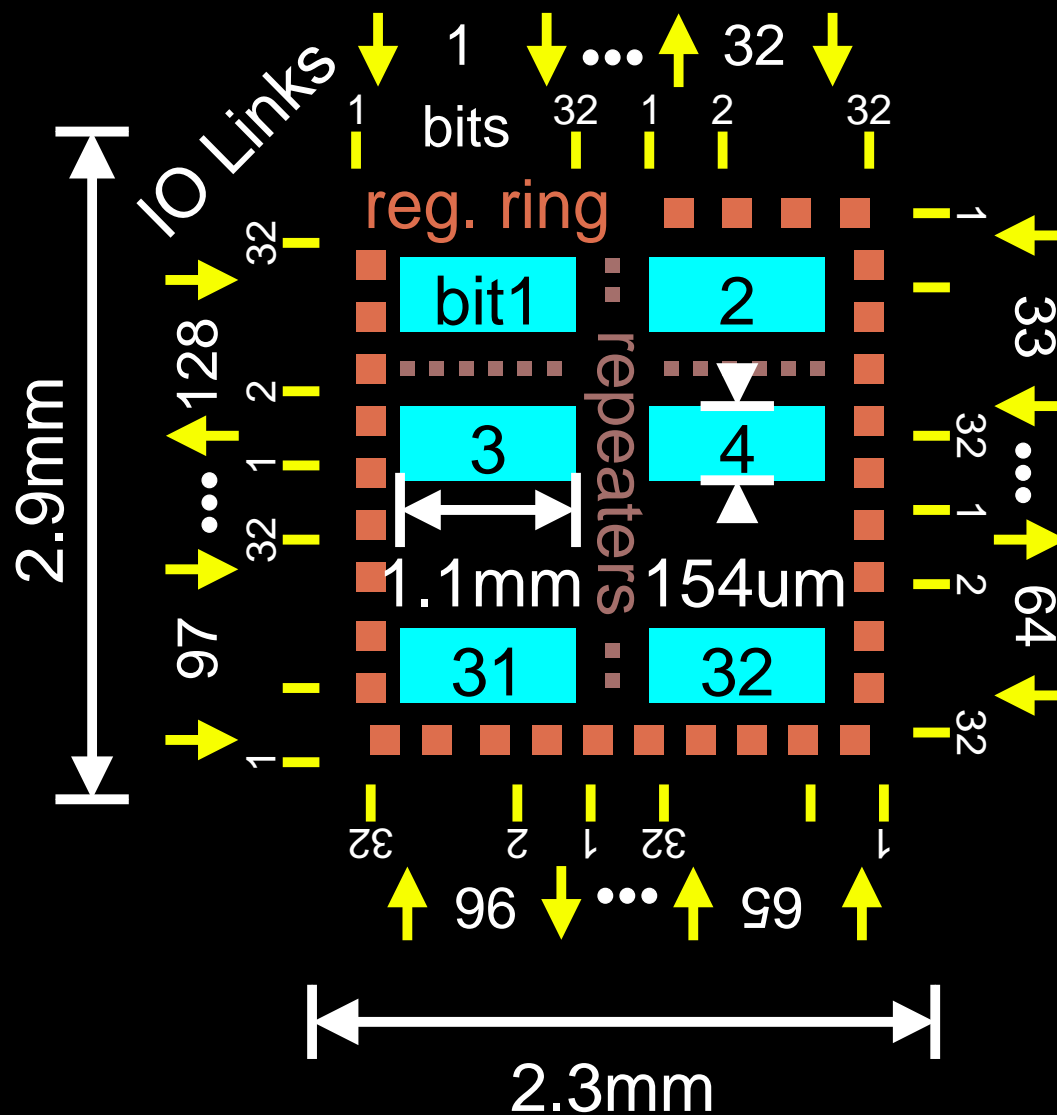
$O(NW)$ wires

Bit Slice Design



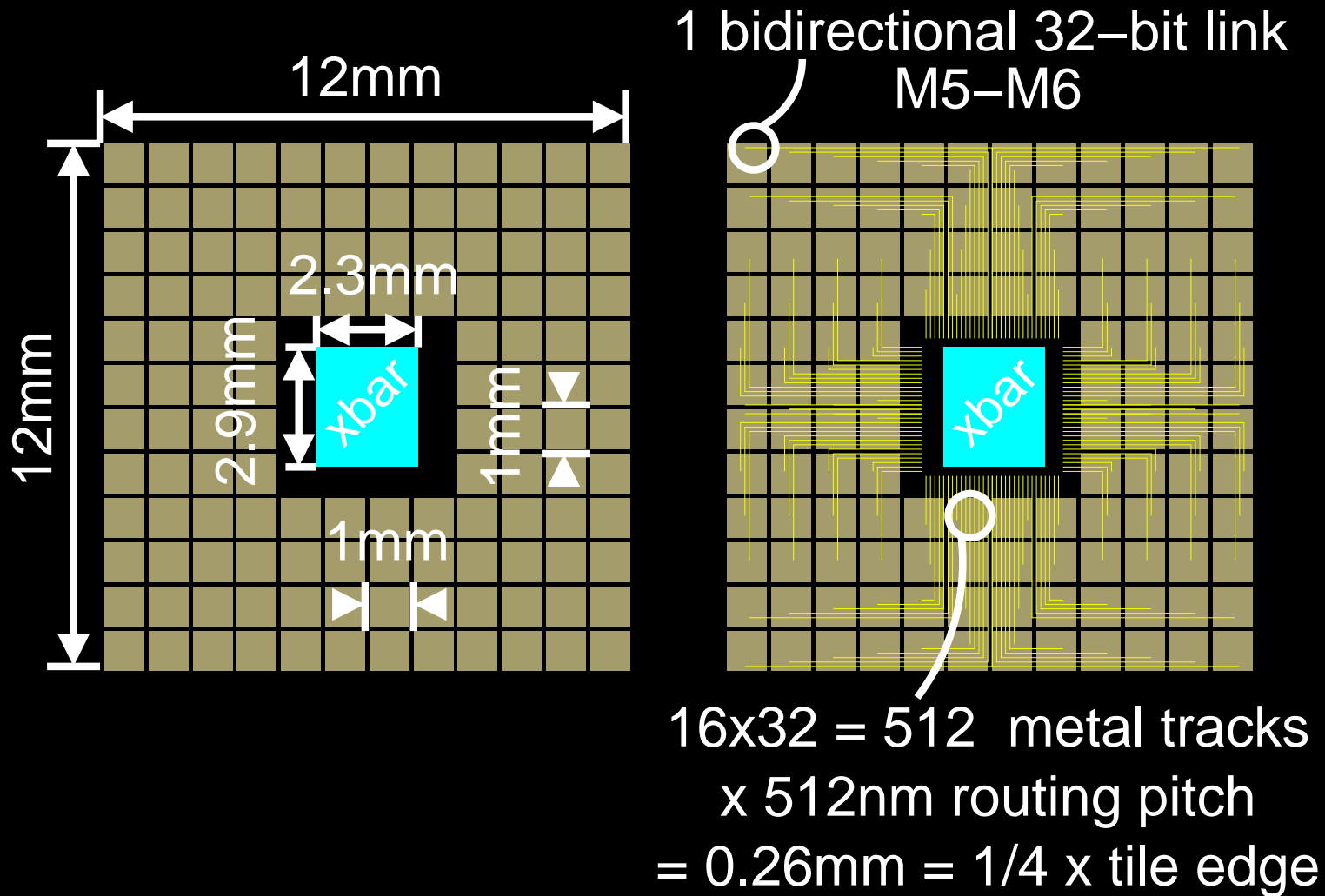
- 90nm CMOS standard cell, M1-M9
- 1.1mm x 154um array of 128 128-to-1 quad-tree muxes
 - wide to provide for quad-tree wiring
- routing in M2-M4 with 95% utilization
- 750MHz worst-case, bounds:
 - NoC frequency at 750MHZ
 - pipelined-link length at 6mm in M5/M6

128x128x24Gb/s Centralized-Crossbar Floorplan



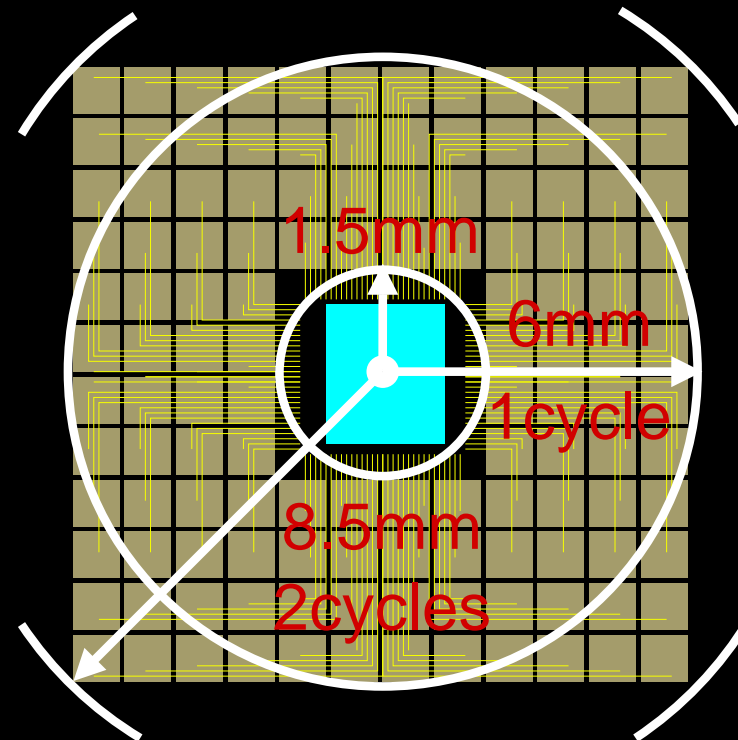
Routed in M5-M8 with 90% area util.
max wire length = halfperimeter < 6mm

128x128x24Gb/s Crossbar-NoC Floorplan



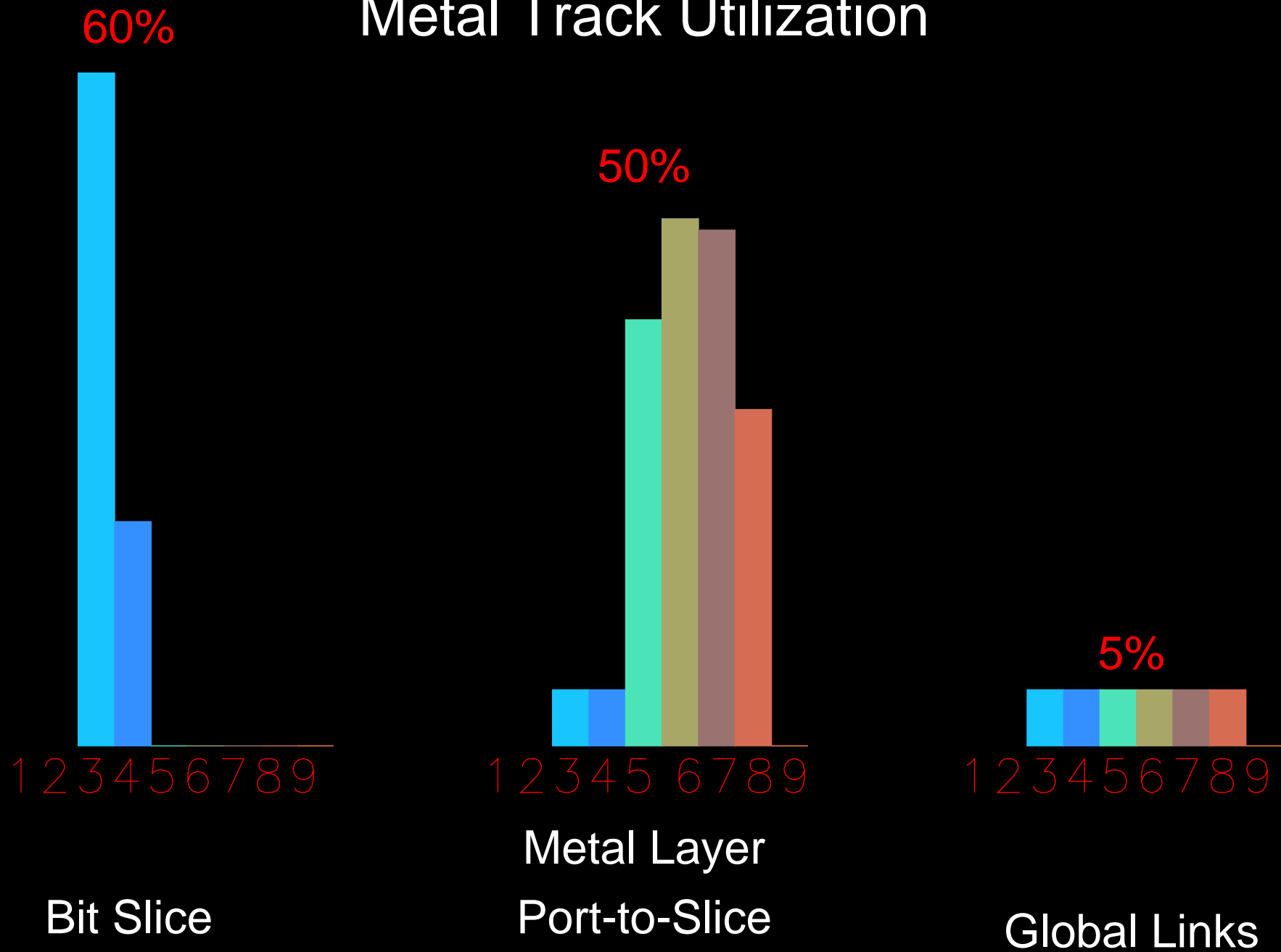
9 sq-mm left for centralized control

7-Cycle Corner-to-Corner Latency



- 2 cycles corner to center (crossbar port)
 - 1 cycle crossbar port to slice
 - 1 cycle slice in to out
 - 1 cycle slice out to crossbar port
- 2 cycles crossbar port (center) to to corner

Metal Track Utilization

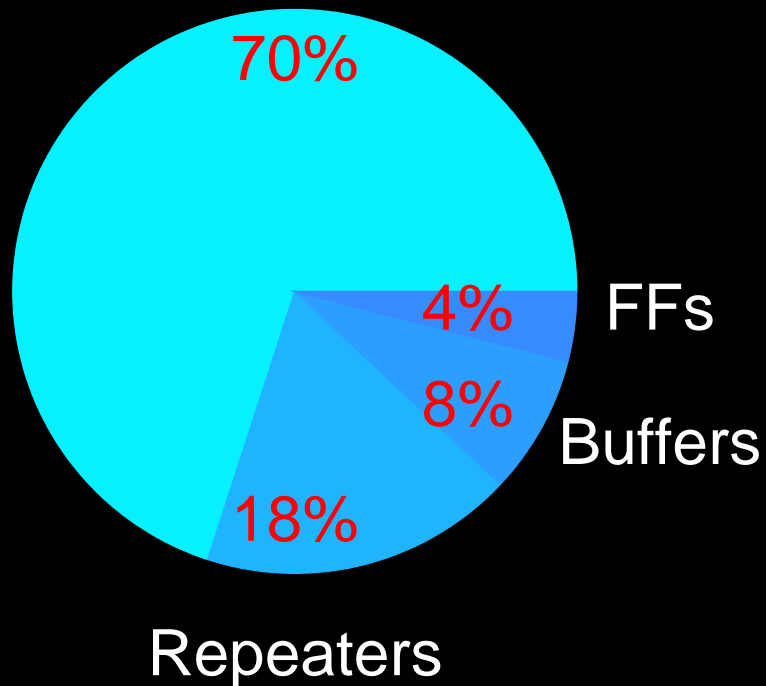


Still plentiful of wiring resources at each level of the circuit hierarchy

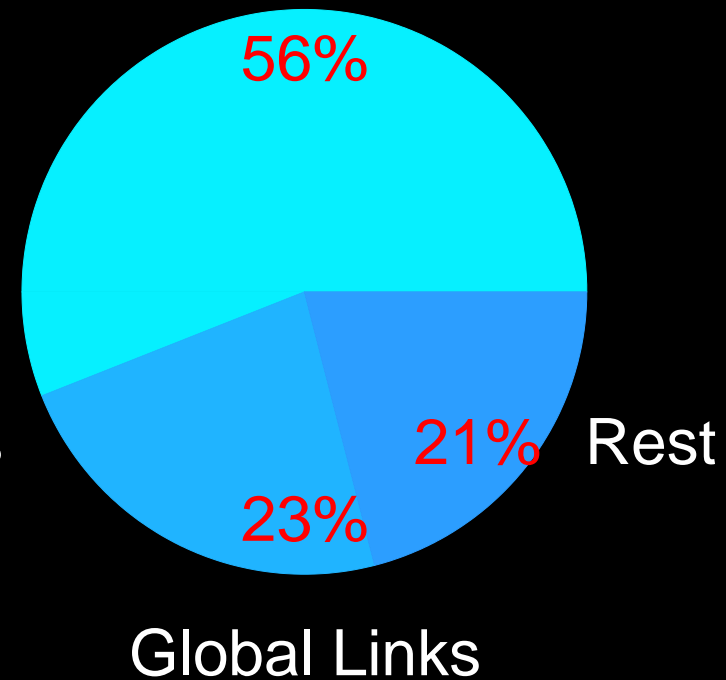
6.6 sq-mm Std-Cell Area

9-Watt Power

Logic Gates (Muxes)



Bit Slices



Traffic: Permutation updated / cycle - toggle rate = 1

Worst-case conditions: 0.9Volts, 750MHz

-- THE END --