

# FORTH-ICS

Computer Architecture & VLSI Systems

### **Energy-Efficient Runtimes for Scalable Multicore Architectures**

## Summary

Power consumption plays an increasingly important role in multicore and manycore processors and systems. As the power cost of cache-coherent shared memory increases disproportionately with the number of cores, research turns towards non cache-coherent architectures that demonstrate better scalability and power efficiency - but also require additional effort to manually program and control the memory hierarchy.

We aim to develop the techniques, tools, algorithms, and software required towards programming languages, runtime systems, and language virtual machines that are specifically tailored for low energy consumption in such architectures, without sacrificing the ease of programming and fast development times provided by a high-level language for such environments.

The Java programming language is the center of our approach, as it is a high productivity language aimed to reduce the expertise required and increase the productivity of the average programmer. Java also targets parallel programming, by supporting a wide range of programming models for parallelism, apart from threads, such as tasks, futures, events, etc. Moreover, it includes a large library of efficient, parallel implementations of popular data structures, that are expected to lie in the heart of multicore applications for the foreseeable future.

By developing a comprehensive library of concurrent data structures and algorithms, and an energy-efficient Java Virtual Machine, this project will advance the state of the art towards easier, more power efficient and scalable concurrent computing. Foundation for Research and Technology Hellas -Institute of Computer Science -Computer Architecture and VLSI Systems (CARV) Laboratory

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